

REMARKS/ARGUMENTS

Claims 1, 2, 5, 7 – 22 remain in this application. Claims 1, 5 and 14 have been amended. Claims 3, 4 and 6 have been canceled.

§ Claim Objections

The Examiner has rejected claim 14 and therefore dependent claims 15 – 22 because claim 14, step g) recited twice “the current time”. Applicants have amended claim 14 to remove the second occurrence of “the current time”. Applicants believe claim 14, and the claims depending from claim 14, are now in condition for allowance.

§ 102 Rejections

The Examiner has rejected claims 1 – 7, and 13 under 35 U.S.C. § 102(b) as being anticipated by Sugaware, et al (US 5,837,026).

The examiner asserts, inter alia, that Sugawara discloses forming at least one semiconductor layer over the glass material by pointing to column 2, lines 30 – 50 of Sugawara.

Applicants respectfully disagree and traverse the rejection.

Applicants point out that, as to claim 6, a fluorescent layer formed on a cathode ray tube for display purposes, as disclosed by Sugawara, is not a semiconductor layer as recited by applicants. Moreover, while Sugawara discloses forming a fluorescent layer on an inner face of the glass panel, Sugawara does not disclose that this is a thermal process, nor does Sugawara disclose using this processing as an input parameter. Indeed, Sugawara discloses that “unnecessary compaction” occurs after the fluorescent layer is formed (column 2, lines 31 – 39) and the formation of the fluorescent layer per se has no bearing on the method taught by Sugawara aside from the need to ensure a correct positional relation between the fluorescent layer and the shadow mask. As regards Applicants’ invention, thermal processing involved in the subsequent formation of a semiconductor layer on the glass material is indeed a consideration that should be factored into the thermal processing of the glass material prior to the semiconductor layer formation.

§ 103 Rejections

The Examiner has rejected claims 8 – 10 under 35 U.S.C. § 103(a) as being unpatentable over Sugawara et al (US 5,837,026) in view of admitted prior art.

Applicants believe the amendment to claim 1 overcomes the rejection. Sugawara does not teach or fairly suggest including input parameters from a subsequent polycrystalline semiconductor deposition process.

The Examiner has rejected claims 11 – 12 under 35 U.S.C. § 103(a) as being unpatentable over Sugawara, et al (US 5,837,026).

For at least the reasons above, applicants believe claims 11 – 12 are patentable over the prior art of record.

Allowable Claims

Applicants note with appreciation the Examiner's observation that claims 14 – 22 would be allowable if rewritten to overcome the objections presented.

Conclusion

Based upon the above amendments, remarks, and papers of records, Applicants believe the pending claims of the above-captioned application are in allowable form and patentable over the prior art of record. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Applicants believe that no extension of time is necessary to make this Reply timely. Should applicant be in error, Applicants respectfully requests that the Office grant such time extension pursuant to 37 C.F.R. § 1.136(a) as necessary to make this Reply timely, and hereby authorizes the Office to charge any necessary fee or surcharge with respect to said time extension to the deposit account of the undersigned firm of attorneys, Deposit Account 03-3325.

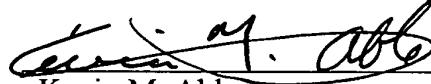
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Please direct any questions or comments to Kevin M. Able at 607-974-2637.

Respectfully submitted,

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CORNING INCORPORATED



Kevin M. Able
Registration No. 52,401
Corning Incorporated
Patent Department
Mail Stop SP-TI-03-1
Corning, NY 14831